PACKET INSTRUCTION DECODER 25 FLAG REGISTER CONTROLLER PROGRAM COUNTER 7 IMMEDIATE VALUE <del>5</del>6 27 EXTERNAL BUS INTERFACE FIG.1 EXTERNAL BUS BUFFER DATA OPERATION PART OPERATION RESULT SELECTOR 21 GENERAL PURPOSE REGISTER MEMORY 2 2 ιū 6 7 က 4 Ξ PROCESSOR SELECTOR PACKET BUS

TRANSMISSION TRANSMISSION INTERFACE TRANSMISSION ..... \_\_\_\_\_\_\_ INTERFACE 9 SWITCH FABRIC PROCESSOR RECEIVING INTERFACE PACKET RELAY APPARATUS 5 Z LAN LAN

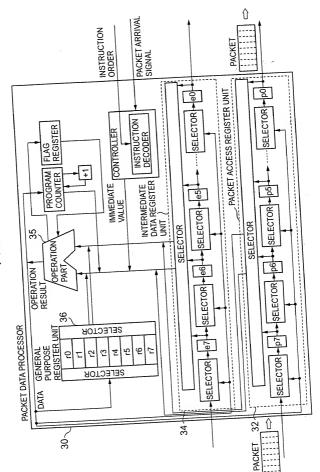
LAN

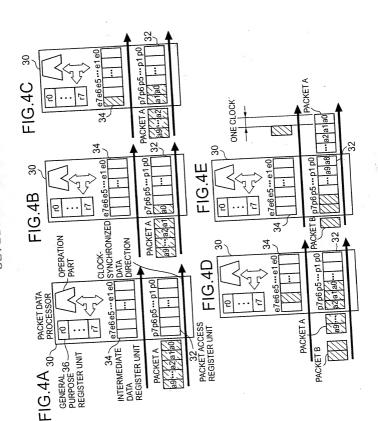
LAN

PN

FIG.2

FIG.3





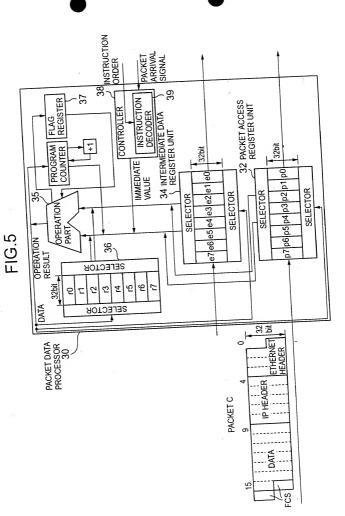
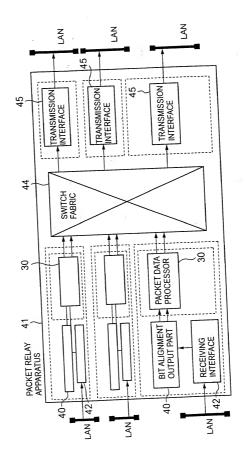


FIG.6



## FIG.7

INSTRUCTION	MNEMONIC	OPERATION					
INSTRUCTION	INSTRUCTION	40					
TYPE		No operation but just clock is executed					
NO OPERATION	NOP	Mars word between registers or memories					
DATA	MOVE	Move lower word (lower bits) between					
TRANSMISSION	MOVW	1 1 1					
	- torm	Move lower byte (lower bits) between					
	MOVB	registers					
	ADD	Add word integers .					
ARITHMETIC	ADC	Add carry and word integer					
OPERATION	ADW	Add lower word					
	AWC	Add lower word and carry					
	SUB	Subtract word integer					
	SBW	Subtract lower word					
	OR	OR operation of word					
LOGICAL	AND	AND operation of word					
OPERATION	14.0	Evaluative-OR operation of Word					
	NOT	operation of Word					
1		NOT (inverse) operation of lower word and					
	NTW	no operation of upper word					
		operation by byte					
	NTB SFL	Shift left to upper byte and fill 0 to					
	SFL	lower byte					
	ROTL	- 1oft					
	SFR	Shift right to lower byte and fill 0 to					
	SFR	upper byte					
	ROTR	tie wie gelat					
		Get first bit '1' position from lower mos					
BIT OPERATION	BSF	l cman operand					
1	BSR	Get first bit '1' position from upper mos					
1	231						
	BT						
1	151	source operand 1. Set result bit to care					
		flag of flag register.					

F1G. 8

			-					IN DACE		
ORDER	INSTRUCTION	SECTION WHICH OF PACKET C IS STORED IN PACKET ACCESS REGISTER UNIT								
NUMBER		p7	p6	p5	p4	p3	p2	p1	p0	
1	ANOP	с0			-		$\dashv$	-	$\dashv$	
2	ANOP	c1	c0			+	-		$\dashv$	
3	ANOP	c2 ·	c1	c0				-+		
4	ANOP	сЗ	c2	c1	c0			$\vdash$	$\dashv$	
5	AMOVE r0 p7	c4	c3	c2	c1	c0		-		
6	AADD r0 r0 p7	C5	c4	c3	c2	c1	<u>c0</u>	-0	-	
7	AADC r0 r0 p7	с6	c5	c4	c3	c2	c1	c0	c0	
8	AADC r0 r0 p7	c7	с6	c5	c4	c3	c2	c1	c1	
9	AADC r0 r0 p7	c8	c7	с6	c5	c4	c3	c2	-	
10	AADC r0 r0 \$0	c9	с8	c7	с6	c5	c4	c3	c2	
11	AMOVE r1 r0	c10	c9	с8	c7	c6	c5	c4	c3	
	ASFR r0 r0 \$16	c11	c10	с9	c8	c7	с6	c5	c4	
12	AADW r0 r0 r1	c12	c11	c10	c9	c8	с7	c6	c5	
13		c13		c11	c10	с9	c8	c7	c6	
14	ANTW r0 r0	c14	-	+	c11	c10	c9	с8	c7	
15	≠MOVE e0 \$1	1101	, 10.0							

38 INSTRUCTION ORDER 39 INSTRUCTION DECODER 37 REGISTER CONTROLLER FLAG 32 PACKET ACCESS REGISTER UNIT PROGRAM 7 32bit IMMEDIATE |p7|p6|p5|p4|p3|p2|p1|p0| 35 SELECTOR SELECTOR OPERATION PART **OPERATION** 36 RESULT SELECTOR ဖ 17 4 Ð ღ 5 DATA SELECTOR ETHERNET DIT HEADER PROCESSOR 301 PACKET DATA CHECKSUM FIELD P HEADER PACKET C DAT/

PACKET ARRIVAL SIGNAL

FIG.9

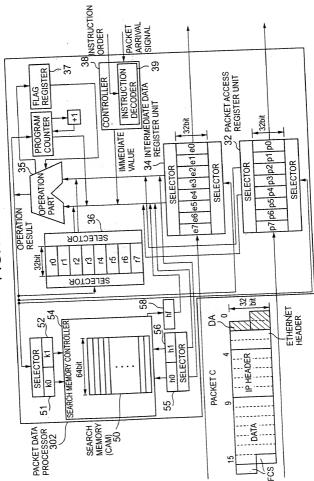
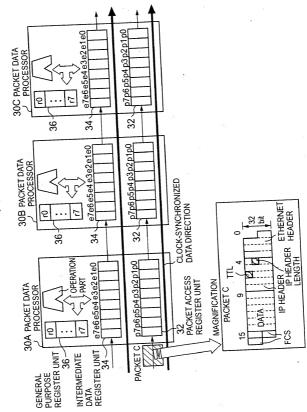


FIG.10





## F I G. 12

INSTRUCTION ORDER OF PACKET DATA PROCESSOR 30A			INSTRUCTION ORDER OF PACKET IDDATA PROCESSOR 30B				NSTRUCTION ORDER OF PACKET NATA PROCESSOR 30C			
SER. NO	ı	ORDER NUMBER	INSTRUCTION	ta	OER JMBER	INSTRUCTION	ORDE	R .	INSTRUCTION	
1	-+	1	ANOP	L			├	+		
	2	2	AMOVE r1 \$0	T			-			
-	3	3	ANOT'r1 r1	1			╁	-		
Г	4	4	ASFR r1 r1 \$24	1			╁	-+-		
$\vdash$	5	5	ASFR r1 p7 \$16	4			╁╴	+		
Г	6	6	AAND r0 r0 r1	4			+-	-		
一	7	7	ASUB r0 r0 \$5	4			+	-+		
r	8	8	<move \$1<="" e3="" td=""><td>4</td><td></td><td>·NOR</td><td>+</td><td>-</td><td></td></move>	4		·NOR	+	-		
Г	9			_	1	ANOP	+	一十		
r	10				2	ANOP	+	-+		
T	11				3	ANOP	+	$-\dagger$		
T	12				4	ANOP AMOVE r0 p7	十			
T	13		3		5	AADD r0 r0 p7	+			
	14				6	AADC r0 r0 p7	十	-		
٢	15			_	7	AADC 10 10 p7	+			
T	16				8	AADC r0 r0 p7	+	1	ANOP	
Ī	17				9	AADC r0 r0 \$0	+	2	ANOP	
Ī	18		100		10	AMOVE r1 r0	十	3	ANOP	
1	19				11	ASFR r0 r0 \$1	6	4	AMOVE r3 \$0	
	20				12	AADW r0 r0 r1		5	ANOT r3 r3	
	21				13	1 1 1 1 1 1 1	_	6	ASFR r3 r3 \$8	
	2	2			14	0.61	_	7	AMOVE r0 p7	
	2	3				711101211		8	ASFR r1 r0 \$24	
	2	4			+-			9	ASUB r1 r1 \$1	
	2	25			+	-		10	=MOVE e3 \$1	
		26		_	+	-		11	ASFL r1 r1 \$24	
		27		_	+	-		12	AAND r0 r0 r3	
		28		_	$\dashv$	-		13	AADD p0 r1 r0	
		29								

FIG. 13

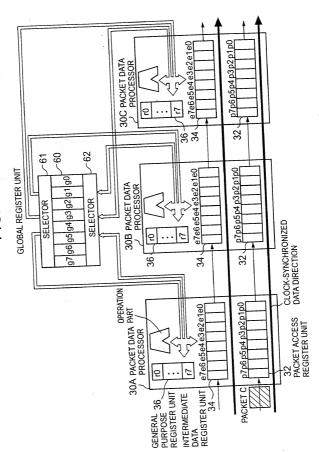
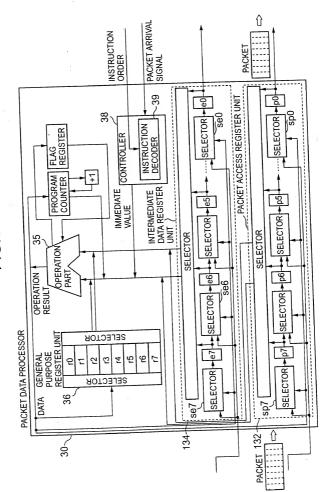
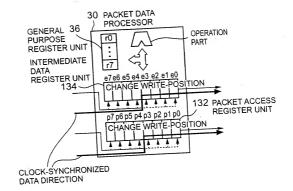


FIG.14



## FIG.15



\_se10 PACKET ACCESS REGISTER UNIT SELECTOR |-- |e0| INSTRUCTION REGISTER IMNEDIATE CONTROLLER DECODER FLAG 7 COUNTER PROGRAM INTERMEDIATE DATA REGISTER SELECTOR 1-165 SELECTOR LNS LNS FIG.16 35 SELECTOR. SELECTOR OPERATION PART SELECTOR 1-1661-OPERATION RESULT 36 PACKET DATA PROCESSOR SELECTOR REGISTER UNIT SELECTOR 1-1671-ဖ ō 77 GENERAL PURPOSE 4  $\varepsilon$ 5 7 SELECTOR PACKET 232

30

234

PACKET ARRIVAL SIGNAL

33

PACKET

SELECTOR 1-100

SELECTOR 1-105

SELECTOR 1-1961

, sp10 ,

SELECTOR

INSTRUCTION ORDER

## FIG.17

